beatrix/bertram SoC [FACT SHEET]

Compact realtime PWM solutions for small FPGAs

The *beatrix* and *bertram* System on Chip (SoC) is a resource saving CPU design for small FPGAs.

It is part of the cCAP (configureable Custom Application Processor) family concept by section5.ch. The cCAP excel in high configureability and low resource usage on FPGA silicon. Independent of the FPGA technology, peripherals and IP cores can be tailored flexibly, starting with low-level register addresses up to number of peripheral instances (such as UART or SPI interfaces) or custom IP cores.

The cCAP family was particularely developed to meet specific requirements of robust and proveable functionality (like for safety relevant environments) while being easy to handle for application programmers at the same time, in order to facilitate handling of FPGA technology. The compact instruction set of the core architecture enables very compact program code as well as customer specific micro code extensions with DSP emulation functionality.

1 Functional overview 'beatrix'/'bertram'

- 32 Bit processor 'ZPUng' v1.1, three stage pipeline @32 Mhz
- Wishbone-Bus for address decoding and peripherals
- Programmable in C (GCC)
- Hardware Debugger (JTAG), GDB

For technical specifications of the standard configuration, see Table 1.

The firmware (Software) in as a bare-metal operating system is typically developed by the application developer using a board supply package library, including the driver for the built-in peripherals. It can be made available in full source code. For custom applications, special IP cores can be integrated easily using a graphical XML register description as shown below.

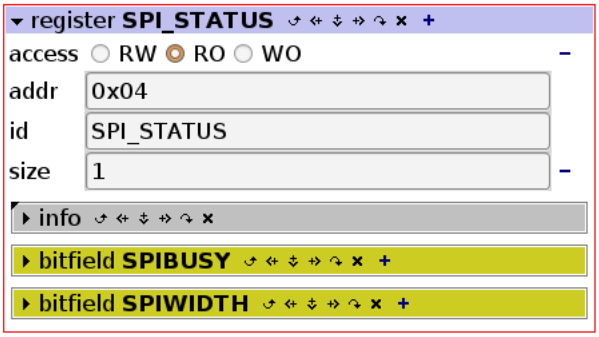


Fig. 1: SPI register description

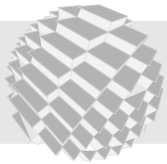
2 Simulation

The entire *beatrix/bertram* SoC can be co-simulated in a virtual machine. Advantages:

- Cycle-accurate verification of correct functionality
- Efficient visual debugging in trace waveforms, optional on-chip trace debugging via Ethernet
- Co-Simulation with Python-Scripts for functional verification

3 Example applications

- Simple configuration processor
- Intelligent UART→LCD-Display
- synchronous Multi-Channel SmartLED-PWM-control
- Redundant Systems (Multi-Core)



Technical specifications		
Memory configuration		
ROM	64kB	Overlay program memory (SPI) read only
L1RAM	8kB	Level one program and data segment
L1CACHE	8kB	Program memory or ROM cache (configureable)
SRAM	1kB	Dedicated Stack Memory
Peripherals		
SCACHE	1	SPI flash cache
SIC	1	System Interrupt Controller with four peripheral channels and configureable priorities
UART	1	UART console
GPIO	2x16	Generic I/O
SYSEXT	1	System extensions: CRC16-accelerator
beatrix specific		
PWM	3	Simple PWM and Timer (System Timer)
LCDIO	1	LCD Interface
bertram specific		
PWMPLUS	3	PWMPlus IP core cycle-accurate real time PWM control, interrupt capable System low latency timer (TIMER0)

Tab. 1: beatrix/bertram standard configuration

4 Reference-Platforms

The b*-SoC-Series are by default available for the following common eval kits:

- Papilio One board
- MACHXO2/3 Breakout Starter Kit

5 Resouce usage

A few resource usage examples are displayed in the tables below. This Spartan3 configuration is using some extra UART buffering that consumes distributed RAM. It can be stripped down to similar logic usage as on the MachXO-Platforms.

Xilinx xc3s250e	
SLICE	2446 (99%)
Slice FF	1854 (37%)
LUT4	4159 (inkl. Distributed RAM) (85%)
RAMB16	12 (100%)

Tab. 2: Resource usage Spartan3

Lattice MachXO2 7000	
SLICE Logic	1197 (35%)
Registers	1772 (25%)
LUT4	2376 (35%)
EBR	20 (77%)

Tab. 3: Resource usage MachXO2

The MACHXO3-6900 usage is almost identical to the MachXO-7000 platform.

6 Further pointers

Overview cCAP-Family
http://section5.ch/index.php/dokumentation/masocist-soc/soc-overview/

Hardware reference `soc-beatrix.pdf`, `soc-bertram.pdf`
See website or contact me directly